SICOLOG, SICOLOG FD

General

The signal converter and data logger *SICOLOG* can acquire signals from its voltage inputs, digital inputs (e.g. frequency signals), serial input (e.g. GPS signals) and logical signal input, and output these signals to a PC, display, voltage output, digital output, and logical signal output. These signals can also be saved onto a USB stick. Additionally, the SICOLOG can also receive and transmit signals from up to two CANs (Controller Area Network) and one LIN (Local Interconnect Network) subbus. Additionally, the *SICOLOG FD* supports also up to two CAN FD.

Before using the signal converter and data logger, it must first be set up by defining a parameter set with the PC program TEMES (which requires a PC with a USB 2.0 port and at least Windows XP), and then by writing this parameter set to a USB 2.0 stick. After making the measurement, the USB stick can be put again into a PC, and the stored data can be written to a PC file for further processing.

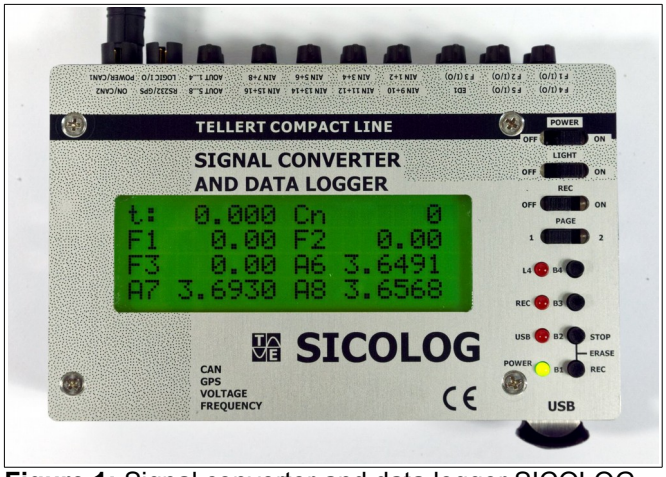

Figure 1: Signal converter and data logger SICOLOG.

Sample Rate

The input signals can be recorded at two different sample rates. The first sample rate is the basic sample rate which can be set to integer multiples of 100 µs, and the second sample rate is an integer multiple of the basic sample rate. The slower second sample rate is 1 to 256 times larger and should also not be larger than 15 s. Note, that a high sample rate of 10 kHz is only working for simple/limited configurations.

The signal converter has a further cycle which runs at a user adjustable rate (with a default value of 10 ms). This cycle is used for CAN signals, LIN signals and calculated signals.

Finally, the SICOLOG has a cycle with a low priority which runs at a fixed rate of 10 ms. This cycle is used for logical input/output signals and display refresh.

Voltage Input Signals

The signal converter can acquire up to 16 voltage signals with a resolution of 12 bits. These signals can be measured within the voltage range from 0 V to 5.12 V where 0 V corresponds to bit value 0, and where 5 V corresponds to bit value 64000 (= 16 × 4000). However, the signals can lie within the range from -30 V to 30 V without a negative impact on other signals. The internal impedance of each voltage input is greater than 10 MΩ.

Each voltage signal input connector has a pin to supply a preamplifier with the operating voltage (decreased by about 1 V) of the signal converter.

The voltage signals are sampled with 10 kHz and represented by the average value over a period of the corresponding sample rate.

If at most 5 voltages are acquired, the voltage signal can optionally be further smoothed with a 4fold averaging. And if at most 14 voltages are acquired, the voltage signal can optionally be further smoothed with a 2fold averaging instead.

Voltage input signals can optionally be linearized via a table look-up during the calculation cycle. For this purpose, user defined characteristic curves are used. Look-up values for input values, which lie between two sample points, are obtained by linear interpolation.

Digital Input Signals

The signal converter has five channels for digital signals:

Frequency Signal: The input voltage level (TTL, CMOS) may lie within the range from 0 V to 20 V. The frequencies to be measured may lie in the range from 0.1 Hz to 100 kHz. Note that the sum over all five input frequencies must not be greater than 100 kHz. The digital signal can be triggered either with the raising edge or the falling edge of the input signal, and is represented by the average value over a period of the sample rate.

Switch State: Depending on the voltage level of the digital input, the digital signal is taken either as bit value 0 or as bit value 1. This signal type can be used for markers or to reset counter readings (see *calculated signals*).

Pulse Width (only the first three digital inputs): The pulse width to be measured may lie in the range from 1 µs to 546 ms. The signal resolution is from 8.333 ns to 8.533 µs (in 9 steps). The digital signal is represented by the average value over a period of the sample rate.

Counter: The 16-bit wrap-around counter is incremented by one after each pulse.

Serial Ports

The signal converter has two serial ports. The first serial port is used for the communication between signal converter and host PC (*RS232*). The 2nd serial port can be used by one of the following items:

GPS receiver: The 2nd serial port can be used to receive NMEA sentences of a GPS receiver. The NMEA receiver supports the messages GGA, VTG and RMC. Following unsigned 16-bit signals can be extracted: Message counter, time (resolution: 0.01 s), speed (resolution: 0.01 kph), height (resolution: 0.1 m; lowest height: 500 m below sea level), number of visible satellites. Following signed 32-bit signals can be extracted: longitude, latitude (with a resolution of 1/600000 degree).

F6 protocol: The 2nd serial port can be used to acquire up to 16 signals via the f6 protocol.

LIN subbus: The 2nd serial port can be used to access a LIN subbus via the optionally available adapter *LIN719/SICO(LOG)*. See also section *LIN*.

Logical Input Signals

The signal converter has three 16-bit input signals, which can be (in groups of 8 bits) fed into the logger over an I²C-bus. For each of the three 16-bit signals a bus address for the lower significant byte, and a bus address for the higher significant byte can be specified. External devices (which are connected to the logger) have bus addresses from 0 to 7.

Logical Output Signals

The signal converter can also output up to three 16-bit signals (in groups of 8 bits). For each of the 16-bit signals a bus address for the lower significant byte, and a bus address for the higher significant byte can be specified. Bus addresses of external devices lie within the range from 0 to 7.

Voltage Output Signals

The signal converter has eight 12-bit-D/A-converter-channels. The output voltage lies within the range from 0 V to 5 V. Each output has an internal impedance of 470 Ω.

Digital Output Signals

If a digital channel is not used as signal input, it can be used as signal output:

Frequency signal ($f_{Min} < f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V. The frequency output may lie within the range from 2 Hz to 100 kHz.

PWM signal ($f_{Min} = f_{Max}$): The output voltage level (TTL, CMOS) is a frequency signal 0 V or 5 V with a frequency of f_{Min}, and a duty cycle depending on the signal source and assignment.

Switch state ($f_{Min} > f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V depending on the signal source and assignment.

CAN

The signal converter can be connected to two CANs (Controller Area Network). Each of the two CAN channels has the ability to receive or to transmit up to 32 CAN messages (with either 11-bit or 29-bit message identifiers). The messages are refreshed during the calculation cycle.

Input signals are embedded within a received message. To extract them, following properties are supported: *start bit* within a message, *bit length* (max. 32 bits), *data type* (*unsigned* or *signed*) and *byte order* (*Intel* or *Motorola*).

The signal converter hardware (physical layer) is compatible to a high speed CAN (which is usually run at 125 kBit/s, 500 kBit/s or 1 MBit/s). An optional adapter integrates the signal converter with a low speed CAN (which is usually run at 83.3 kBit/s, 100 kBit/s or 125 kBit/s).

Note, that each of the two ends of a high speed CAN must be terminated (typically with a 120 Ω resistor between *CAN_H*-wire and *CAN_L*-wire).

If the CAN signals can be assigned freely, then following rules should be followed in order to reduce the computational complexity:

- Choose Intel as byte-alignment
- Choose 16-bit or 32-bit as data type
- DWORD-align the start bit: 0, 32. If not possible, then WORD-align the start bit: 0, 16, 32, 48. (If not possible, then try BYTE-alignment: 0, 8, 16, 24, 32, 40, 48, 56.)
- Avoid further linear transformations

CAN FD

The SICOLOG does not support a CAN FD. The SICOLOG FD on the other hand supports additionally up to two CAN FD. See section SICOLOG FD for further information.

Another method to access a CAN FD is a CAN FD router which maps the CAN FD messages to a CAN, like PCAN Router FD from PEAK-System Technik GmbH.

LIN

The 2nd serial port of the SICOLOG can be used over the optionally available adapter LIN719/SICO(LOG) to access a LIN subbus (Local Interconnect Network). It can be configured to work either as a master control unit or as a slave control unit. The SICOLOG can receive or transmit up to 8 LIN messages. The messages (to be received or to be transmitted) are refreshed during the calculation cycle.

Input signals are embedded within a received message. To extract them, following properties are supported: start bit within a message, bit length (max. 32 bits), data type (unsigned or signed) and byte order (Intel or Motorola). Multiplex signals are only supported for message reception (and not for transmission).

However, the SICOLOG ignores bus-sleep-requests and wake-up-signals.

As master control unit, the SICOLOG supports one schedule table with up to 16 identifier-delay-entries (where the delay must be an integer multiple of the calculation cycle time).

If the LIN signals can be assigned freely, then following rules should be followed in order to reduce the computational complexity:

- Choose Intel as byte-alignment
- Choose 16-bit or 32-bit as data type
- DWORD-align the start bit: 0, 32. If not possible, then WORD-align the start bit: 0, 16, 32, 48. (If not possible, then try BYTE-alignment: 0, 8, 16, 24, 32, 40, 48, 56.)
- Avoid further linear transformations

Calculated Signals

The signal converter supports operations with signal values. For this purpose the signal values are treated as signed 32-bit integer values with little-endian (= Intel) byte order. Following operations are already built in the firmware: constant value; basic arithmetic (sum, difference, product, ratio); bit manipulations (AND, OR, XOR, mirror bits, byte order change from Intel to Motorola and vice versa); comparisons (=, <, ≤); condition (use signal s_1 if condition is true, otherwise use signal s_2); delay (e.g. for derivation or signal filtering); counter operations (e.g. for 32-bit-counters or for integration).

More complex operations can be obtained by using the result of a single operation as an operand for following operations.

Power Control

The signal converter should never be powered off by suddenly breaking the supplying voltage while it is recording (indicated by the *REC* LED). Instead, it should be powered off either manually with the power slider, or automatically by removing the power control signal from connector *ON/CAN2*. (However, the file access, while not preallocating, is designed in a way that the signal converter can be powered off by a sudden break, and the file structure remains healthy, but usually loosing at most 5 seconds of the recording: maximal 1 s for the prophylactic saving and usually maximal 4 s for a full file cache.)

By turning off the power slider, while the signal converter is recording, first a stop event is created, and then (after this stop event has been processed) the signal converter is powered off after the file cache is empty (because the signal converter is no longer recording).

When using the *ON/CAN2* connector to control the power state of the signal converter, the power slider should be left turned off.

An ongoing recording after the stop event can be stopped forcibly by turning the *REC* slider off.

Recording Control

Note that a measurement can only be erased with holding the buttons *B1* and *B2* down after the *REC* slider has been turned off. If there exists a measurement, then the *L4* LED is lit for about two seconds, and when it automatically extinguishes (with unchanged button states), also the measurement is erased.

Trigger Conditions

The signal converter supports up to four trigger conditions. If one condition changes from not satisfied to satisfied, it generates either a start or a stop event. The condition is always a comparison of an input signal with a constant threshold value. Calculated signals can be used to obtain a more complex trigger.

Display

The LCD (liquid-crystal display) has four lines with 20 alphanumeric characters per line. The LCD is considered as a 4×2 matrix with 8 cells and 10 characters per cell. Each cell shows one of the following display items: static text; signal value (either as fixed point value, hexadecimal value or binary value), status information (like CPU load), or date and time.

The user can switch the display to a second set of items, and re-initialize the display, with the *1-2 slider*.

A user-defined text can be displayed for a few seconds during the start-up of the signal converter (or when the displayed items are changed via the *1-2 slider*). This can for example be used to display the name of the parameter set or the device number.

Real Time Clock

The signal converter has a built-in real time clock. A 32-bit time stamp is derived from current date and time with a resolution of 1 s. This time stamp represents the seconds from the beginning of the year 1970 to the actual point in time.

If, however, the real time clock is not available, the time stamp is set to zero. Note, that the real time clock is not automatically adjusted for daylight saving changes.

Multiplexer Support

In order to control multiplexed input signal sources, the signal converter can broadcast the next control byte to connected multiplexers over its logic I/O port just after storing its signal values during the fast or slow recording cycle. This synchronization minimizes signal crosstalk between two neighboring channel time slices since the command to switch to the next channel is sent as soon as possible. The list of control bytes contains 16 items, where the 4 least significant bits of a control byte represent the channel number, and where the 4 most significant bits of a control byte can be used for the corresponding operation range.

Signal crosstalk can be further reduced or even entirely avoided by defining a duration during which the SICOLOG ignores the voltage input signal while the

multiplexer shifts to the next channel. This duration should include the max. duration for broadcasting the control byte (2.5 ms), possible switch times (e.g. 3.5 ms for thermocouple amplifier *TH16MI*) and transient times for the multiplexer. This yields a recommended suppression duration of 20 ms for thermocouple amplifier *TH16MI.*

The channel number (0...15) is copied to the four least significant bits of the input signal. This allows to record only the multiplexed signal and to assign its signal values to the corresponding channels afterwards.

Technical Data

Power supply:	8 V to 30 V DC
Current consumption without USB stick (@ 12 V DC):	with lighted display: ca. 200 mA with unlighted disp.: ca. 90 mA
Sample rate:	1 ms (with limited abilities: 100 µs) or slower
CAN bus:	ISO11898-1 compliant
USB:	USB 2.0 Full Speed
Box size without plugs, sockets, buttons and sliders:	120 mm × 75 mm × 32 mm
Weight:	0.315 kg

PC Software

The signal converter can be set up with the PC software TEMES. TEMES requires a PC with a USB 2.0 port and at least Windows XP. The current version can be downloaded from the Internet (http://tellert.de/?product=TEMES).

Further functions of TEMES are:

- **Online-Calibration:** The voltage input signals can be calibrated either at one known point (offset adjustment) or at two known points (two-point calibration).
- **Online-View:** The online-view displays a curve chart of the current signal values in the upper part of the window. The lower part of the window is used to display these values as numbers in physical units.
- **Saving Measurements:** The measurements, which are captured by the SICOLOG, can be stored to a PC file. After storing the data, the measurement can directly be displayed as a curve chart.
- **Exporting Measurements:** A measurement can (via a provided and documented DLL interface) be exported to ASCII, MDF3, M, SCE, JL and R file format. This DLL also allows programmers to read TEMES measurement files without knowing the internal file structure (http://tellert.de/?product=til).

Following TEMES functions require an optional available single-PC license:

- **Import of ASCII files:** Measurements can be imported from ASCII files.

Scope of Supply

The delivery of a signal converter SICOLOG includes:

- SICOLOG box
- USB stick
- 4-pin-cable for power supply (12 V DC) and CAN with open wire ends
- PC-connection cable with either a USB plug or a 9-pin SUB-D-socket
- PC-software (TEMES, which requires a computer with a USB 2.0 port and at least Windows XP)

Optional Accessories

General accessories:

- Power transformer (Euro plug; 100-230 V AC; 50-60 Hz)
- Low speed CAN adapter *LCC719* (to connect the SICOLOG to a low speed CAN)
- Power-off delay *POD8*

Accessories for digital input:

- Hall effect sensor *HS-M10X1* (to detect passing magnets)
- Hall effect sensor *FPS* (to measure the frequency of steal teeth wheels)
- Preamplifier *PP1* for AC-coupled signals (for magnetic sensors)

Accessories for voltage input:

- Differential Input Amplifier *DIA1/DIA2*
- DC-bridge amplifier *DCBA1ME/DCBA2ME*
- Temperature sensor *PT100M/PT1000M*
- NTC temperature sensor *NTC10K* (operating point 25 °C) and *NTC2K* (operating point 66 °C) for temperatures from –40 °C to 150 °C
- Thermal sensor amplifier *TH1M/TH2M*
- Galvanically isolated thermal sensor amplifier *TH16MI* or *TH16MI/CAN* (16 channels, multiplexed)

Accessories for logical signals:

- Input for eight logical signals *LI8M*
- Output for eight logical signals *LO8M*

Accessories for the RS232 connector:

- GPS receiver *HS10G/HS16G* or *GPS10G/GPS16G*
- External display *ED12*
- LIN adapter *LIN719/SICO(LOG)*

Accessories for the ED1 connector:

- External display *ED9*

USB Stick

The USB 2.0 stick (whose size should be no more than 2 TiB) has to be formatted either with one partition of FAT16 (with 512 bytes per sector) or with one partition of FAT32 (with 512 bytes per sector).

When a fresh USB stick is inserted, the SICOLOG first preallocates almost all clusters, and also creates the file

\TELLERT\SICOLOG\CONFIG.TSF

During the preallocation, communication is impossible. The preallocation phase must also not be interrupted, otherwise the stick needs to be formatted again, and the preallocation must be started again.
As soon as measured data is available, the stick must not be defragmented because cluster numbers are stored in the data files for faster access.
A USB stick needs to be *ejected* before it is unplugged from the PC (in order to keep the FAT16 or FAT32 file system healthy). TEMES has a checkbox for ejecting a USB stick automatically (see the corresponding mass storage dialog boxes), otherwise the USB stick needs to be ejected manually (e.g. with the context menu of the Windows Explorer).

Note that the *REC* LED should be unlit if you remove the power from connector *POWER/CAN1*. See section *Power Control* for further information.

For performance reasons, it is recommendable to use at least a USB 3.0 stick.

Multiple Configurations

The SICOLOG's internal configuration memory has a size of 63 KiB which can hold up to 200 different configurations. The storage location is deferred onto a USB stick as soon as a USB stick is inserted.

The configuration menu is accessed with pressing button B3 for a longer time. Then, the text "*1/1 I" is displayed where the star indicates the currently selected configuration, the first number represents the selectable configuration, the last number represents the number of stored configurations and the "I" indicates the storage location (*I* = internal, *E* = external / USB stick). With a short keypress of B3, the next configuration is selected. And with a longer keypress of B3 the configuration is finally selected.

By pressing B4, the currently selected configuration is copied. And by longer pressing B4 (for at least 4 seconds), the LED L4 is lighted and after 4 seconds when it automatically extinguishes, the currently selected configuration is deleted.

The configuration menu is disabled as soon as measurement data is available.

Splash Water Protection Option

There is an option available which protects the SICOLOG from splash water.

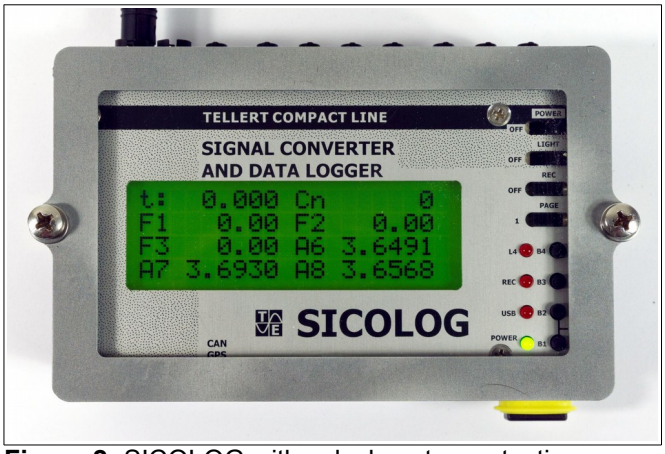

Figure 2: SICOLOG with splash water protection.

Performance

24-hours-recordings onto a SanDisk Ultra Fit 32 GB USB 3.0 stick, without loosing a sample, are listed as follows (Note, that the overhead of one sample is two bytes in these cases):

Sample rate [ms]	Number of 16-bit channels	Size [GiB]	Speed [KiB/s]
0.1	3	6.4	78
0.2	8	7.2	88
0.3	12	7.0	85
0.4	18	7.6	93
0.5	23	7.7	94
1	51	8.4	102

When the SICOLOG is too slow to write the signals onto the USB stick in time, the SICOLOG stops the measurement and waits until its internal 400-KiB-cache is written onto the USB stick before restarting the measurement with an additional timestamp and a mention in the TEMES variable *Measurement.M1.exceptions*. The duration of lost samples (between measurement stop and start) is usually maximal 4 seconds.

The settings of working online TEMES charts are listed as follows:

Sample rate [ms]	Number of 16-bit channels		Speed [KiB/s]
0.2	1		9.8
0.3	2		13
0.4	3		15
0.6	4		13
0.7	5		14
0.8	6		15
0.9	7		15
1.1	8		14
2	15		15

2.1	16		15
5	38		15
10	77		15

Encryption

The SICOLOG does not support the SICOLOG encryption. But there is a variant of the SICOLOG available (on request), namely the *SICOLOG E-Edition*, which supports encryption with a key length of 56 bits.

SICOLOG FD

The SICOLOG FD supports additionally up to two CAN FD. Each CAN FD channel is limited to 8 Mbps, 2 KiB RAM and no support for remote frames. The additional current consumption is about 10 mA per used CAN FD channel (at 12 V).

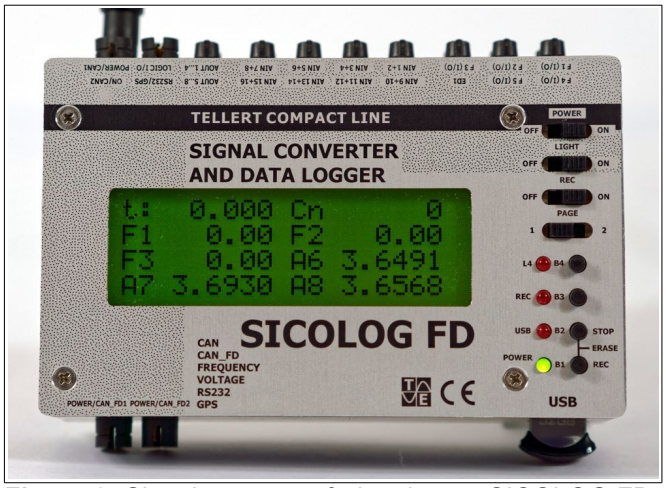

Figure 3: Signal converter & data logger SICOLOG FD.

Each of the two CAN FD channels has the ability to receive or to transmit up to 31 CAN FD messages (with either 11-bit or 29-bit message identifiers). The messages are refreshed during the calculation cycle.
Input signals are embedded within a received message. To extract them, following properties are supported: *start bit* within a message, *bit length* (max. 32 bits), *data type* (*unsigned* or *signed*) and *byte order* (*Intel* or *Motorola*).

Note, that each of the two ends of a CAN FD must be terminated (typically with a 120 Ω resistor between *CAN_H*-wire and *CAN_L*-wire).

If the CAN FD signals can be assigned freely, then following rules should be followed in order to reduce the computational complexity:

- Choose Intel as byte-alignment
- Choose 16-bit or 32-bit as data type
- DWORD-align the start bit: 0, 32, … If not possible, then WORD-align the start bit: 0, 16, 32, 48, ... (If not possible, then try BYTE-alignment: 0, 8, 16, 24, 32, 40, 48, 56, ...)
- Avoid further linear transformations

POWER/CAN_FD1: This plug supplies the signal converter with voltage and connects the signal converter to CAN_FD1.

Pin	Assignment	Old Wire Color	Wire Color
1	Supplying voltage U_B (8 V to 30 V DC inverse-polarity protected)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN_FD1)	Black	Blue
4	CAN_H (CAN_FD1)	Orange	Black

POWER/CAN_FD2: This plug supplies the signal converter with voltage and connects the signal converter to CAN_FD2.

Pin	Assignment	Old Wire Color	Wire Color
1	Supplying voltage U_B (8 V to 30 V DC inverse-polarity protected)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN_FD2)	Black	Blue
4	CAN_H (CAN_FD2)	Orange	Black

More Information (Internet)

The SICOLOG homepage is available at:

http://www.tellert.de/?product=sicolog

Pin Assignment

The sockets and plugs of the SICOLOG are manufactured by *Binder* and parts of *Binder Series 719*. The socket pins (in front view) are numbered clockwise starting with the first pin after 12 o'clock position. The plug pins are numbered correspondingly anti-clockwise. The first pin is respectively labeled at the solder side (back view).

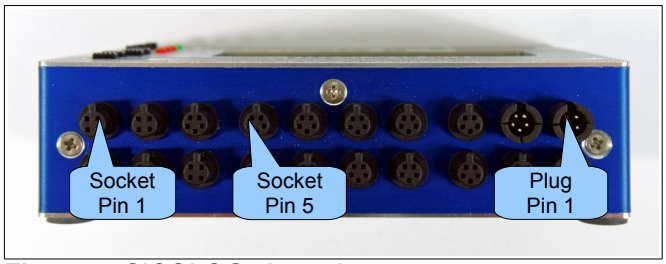

Figure 4: SICOLOG pin assignment.

POWER/CAN1: This plug supplies the signal converter with voltage and connects the signal converter to CAN1.

Pin	Assignment	Old Wire Color	Wire Color
1	Supplying voltage U_B (8 V to 30 V DC inverse-polarity protected)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN1)	Black	Blue
4	CAN_H (CAN1)	Orange	Black

ON/CAN2: This plug provides a power control input and connects the signal converter to CAN2.

Pin	Assignment	Old Wire Color	Wire Color
1	Power control input (8 V to 30 V DC)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN2)	Black	Blue
4	CAN_H (CAN2)	Orange	Black

RS232/GPS: This plug provides two serial ports.

Pin	Assignment	9-pin SUB-D plug of host PC
1	TX1	Pin 2
2	Ground	Pin 5
3	RX1	Pin 3
4	U_L or TX2	
5	RX2	

LOGIC I/O: This socket provides access to the I²C bus for logical input and output signals.

Pin	Assignment
1	Limited supplying voltage U_L
2	Ground
3	SDA (serial data line)
4	SCL (serial clock line)

AOUT1...4, AOUT5...8: These sockets provide outputs for the voltage output signals.

Pin	Assignment
1	Analog output 1 / 5: 0...5 V, R_i = 470 Ω
2	Analog output 2 / 6: 0...5 V, R_i = 470 Ω
3	Analog output 3 / 7: 0...5 V, R_i = 470 Ω
4	Analog output 4 / 8: 0...5 V, R_i = 470 Ω
5	Ground

AIN1+2, ..., AIN15+16: These sockets provide inputs for the voltage input signals.

Pin	Assignment U_L
1	Limited supplying voltage U_L
2	Ground
3	Analog input 1 (...15)
4	Analog input 2 (…16)
5	5.12 V reference voltage (max. 50 mA for AIN1+2...AIN15+16)

ED1: This socket provides access to the I²C bus for the display.

Pin	Assignment
1	Limited supplying voltage U_L
2	Ground
3	AOUT1
4	SDA (serial data line)
5	SCL (serial clock line)

F1 (I/O), ..., F5 (I/O): These sockets provide a connection to the digital (frequency) signals.

Pin	Assignment
1	Limited supplying voltage U_L
2	Ground
3	Digital input 1 (…5) connected over 100 kΩ to 5 V
4	Frequency output

U_L = U_B - 1...2 V, limited to 12.5 V (regulated).

Note that the sum of the currents which are drawn from U_L must be less than or equal to 300 mA.

